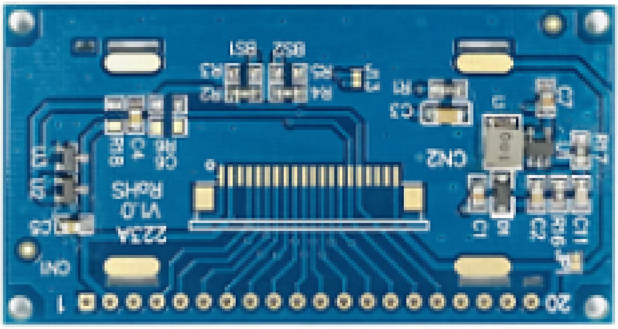
DG-223B OELD

LCD MODULE USER MANUAL



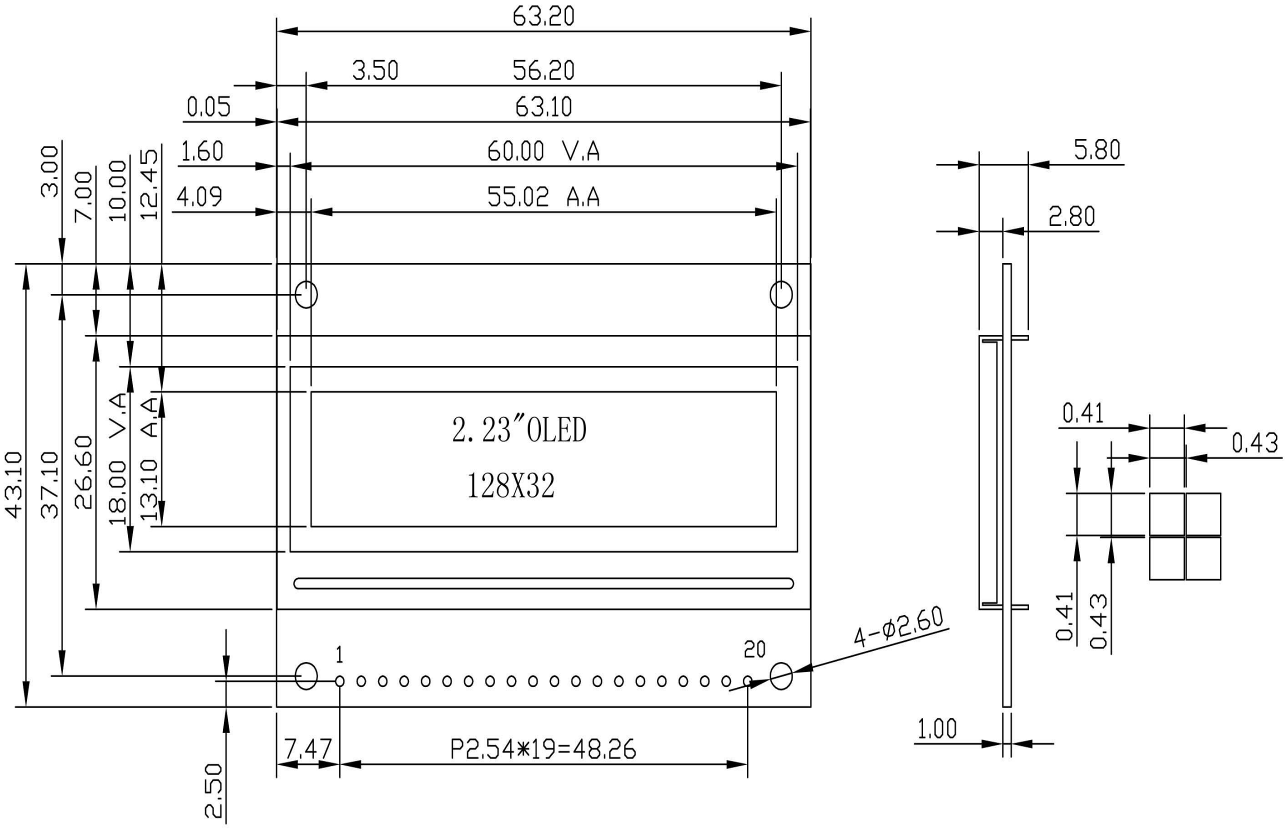
1. FUNCTIONS & FEATURES

Features
- 128X32 dots
- Font Color:YELLOW/WHITE/GREEN
- Driver IC:SSD1305
- 8-BIT 68XX/80XX Parallel,4-wire SPI,I2C

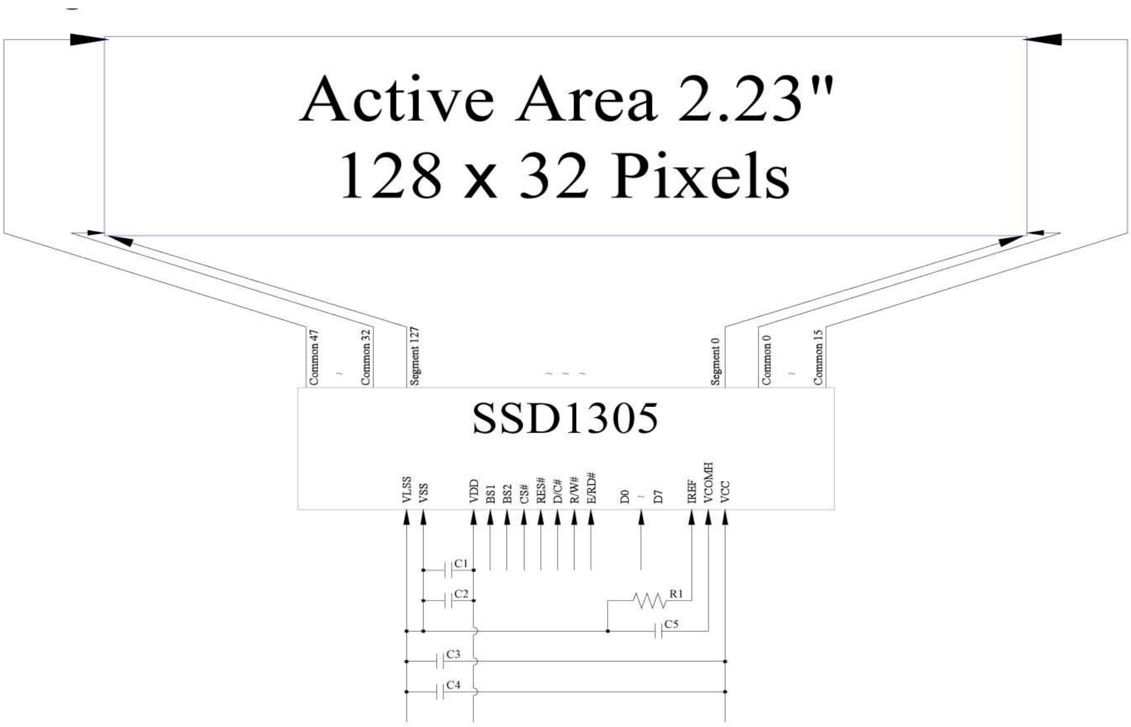
2. MECHANICAL SPECIFICATIONS

ITEM	SPECIFICATIONS	UNIT
Module Size	63.2L×43. 1W×5. 8H	mm
View Area	60×18	mm
Effective Area	128×32	dots
Dot Size	0.39×0.39	mm
Dot Pitch	0.43×0.43	mm

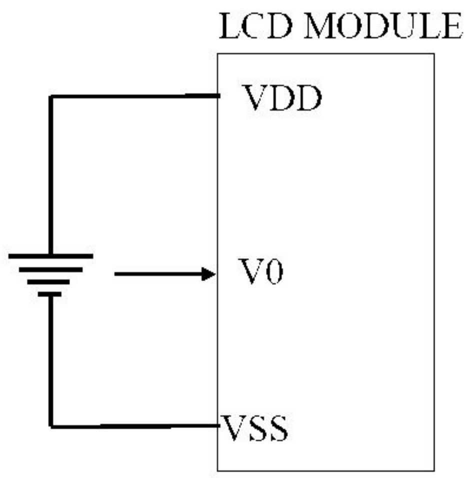
3. EXTERNAL DIMENSIONS



4. BLOCK DIAGRAM



5. POWER SUPPLY



6. PIN DESCRIPTION

6.1 J1 PIN DESCRIPTION

Parallel Interface(8080):

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3V	Power Supply For Logic
3	NC	-	No connect
4	D/C(RS)	H/L	H：Data　L：Command
5	WR	H/L	8080:Active LOW Write signal
6	RD	H/L	8080: Active LOW Read signal
7～14	D0～D7	H/L	Data Bus
15	GND	0V	Power Ground
16	/RST	H/L	Active LOW Reset signal
17	/CS	L	Chip Select
18	GND	0V	Power Ground
19	BS2	+3.3V	Power Supply For Logic
20	BS1	+3.3V	Power Supply For Logic

Parallel Interface(6800):

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3V	Power Supply For Logic
3	NC	-	No connect
4	D/C(RS)	H/L	H：Data　L：Command
5	WR	H/L	6800:Read/Write select signal, R/W=1: Read R/W: =0: Write
6	RD	H/L	6800:Operation enable signal. Falling edge triggered.

7～14	D0～D7	H/L	Data Bus
15	GND	0V	Power Ground
16	/RST	H/L	Active LOW Reset signal
17	/CS	L	Chip Select
18	GND	0V	Power Ground
19	BS2	+3.3V	Power Supply For Logic
20	BS1	0V	Power Ground

4-SPI

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3V	Power Supply For Logic
3	NC	-	No connect
4	D/C(RS)	H/L	H：Data　L：Command
5	WR	0V	Power Ground
6	RD	0V	Power Ground
7	SCLK(D0)	H/L	Serial Clock signal
8	SDIN(D1)	H/L	Serial Data input signal
9	NC(D2)	-	No connect
10～14	D3～D7	0V	Power Ground
15	GND	0V	Power Ground
16	/RST	H/L	Active LOW Reset signal
17	/CS	L	Chip Select
18	GND	0V	Power Ground
19	BS2	0V	Power Ground
20	BS1	0V	Power Ground

I2C Interface:

ITEM	SYMBOL	LEVEL	FUNCTION
1	GND	0V	Power Ground
2	VDD	+3.3V	Power Supply For Logic
3	NC	-	No connect
4	SA0(D/C)	H/L	Slave Address Selection signal
5	WR	0V	Power Ground
6	RD	0V	Power Ground
7	SCLK(D0)	H/L	Serial Clock signal
8	SDIN(D1)	H/L	Serial Data input signal (pins 8 and 9 can be tied together).
9	SDIN(D2)	H/L	Serial Data output signal (pin9 can be no connect).
10～14	D3～D7	0V	Power Ground
15	GND	0V	Power Ground
16	/RST	H/L	Active LOW Reset signal
17	/CS	L	Chip Select
18	GND	0V	Power Ground
19	BS2	0V	Power Ground
20	BS1	+3.3V	Power Supply For Logic

MPU Interface Pin Selections

Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	Serial Interface	I2C Interface
BS2	1	1	0	0
BS1	0	1	0	1

MPU Interface Pin Assignment Summery

Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	D/C	/RES
I2C	Tie LOW					SDA_{IN}	SDA_{OUT}	SCL	Tie LOW			SA0	/RES

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	Vdd	2.4	3.6	V	1, 2
Supply Voltage for Display	Vcc	0	15	V	1, 2
Operating Temperature	Top	-30	85	℃	-
Storage Temperature	Tst	-40	90	℃	-

Note 1: All the above voltages are on the basis of “VSS = 0V”.
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

9 . ELECTRICAL CHARACTERISTICS

Items	**Symbol**	**Condition**	**Min**	**TYP**	**Max**	**Unit**
Operating Temperature Range	Top	Absolute Max	-40	—	+85	C
Storage Temperature Range	Tst	Absolute Max	-40	—	+90	C
Supply Voltage	Vdd		3.0	3.3	3.6	V
Supply Current (logic)	Idd	Ta=25°C, VDD=3.3V	—	180	300	µA
Supply Current (display)	ICC	50% ON, VDD=3.3V	—	62	70	mA
		100% ON, VDD=3.3V	—	113	120	mA
Sleep Mode Current	IDD+ICCSLEEP		—	3	15	µA
“H” Level input	Vih		0.8*VDD	—	VDD	V
“L” Level input	Vil		VSS	—	0.2*VDD	V
“H” Level output	Voh		0.9*VDD	—	VDD	V
“L” Level output	Vol		VSS	—	0.1*VDD	V

Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Top	AV		—	80	—	
Viewing Angle – Bottom	AV		—	80	—	
Viewing Angle – Left	AH		—	80	—	
Viewing Angle – Right	AH		—	80	—	
Contrast Ratio	Cr		2000:1	—	—	—
Response Time (rise)	Tr	—	—	10	—	us
Response Time (fall)	Tf	—	—	10	—	us
Brightness		50% checkerboard	100	120	—	cd/m2
Lifetime		Ta=25°C, 50% checkerboard	10,000	—	—	Hrs

Note: Lifetime at typical temperature is based on accelerated high - temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until Half - Brightness. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn﹣in) images may occur. To avoid this, every pixel should be illuminated uniformly.

Built﹣in SSD1305 controller.

Instruction Table

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set Lower Column Start Address	0	**00~ 0F**	**0**	**0**	**0**	**0**	**X3**	**X2**	**X1**	**X0**	Set the lower nibble of the column start address register for Page Addressing Mode.	0
Set Higher Column Start Address	0	**10~1F**	**0**	**0**	**0**	**1**	**X3**	**X2**	**X1**	**X0**	Set the higher nibble of the column start address register for Page Addressing Mode.	0
Set Memory Addressing Mode	0	**20** **A[1:0]**	**0** *****	**0** *****	**1** *****	**0** *****	**0** *****	**0** *****	**0** **A1**	**0** **A0**	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode A[1:0] = 11b, Invalid	10b
Set Column Address	0	**21** **A[7:0]** **B[7:0]**	**0** **A7** **B7**	**0** **A6** **B6**	**1** **A5** **B5**	**0** **A4** **B4**	**0** **A3** **B3**	**0** **A2** **B2**	**0** **A1** **B1**	**1** **A0** **B0**	Setup column start and end address A[7:0]: Column start address. Range: 0-131d B[7:0]: Column end address. Range: 0-131d	0 131d
Set Page Address	0	**22** **A[2:0]** **B[2:0]**	**0** ***** *****	**0** ***** *****	**1** ***** *****	**0** ***** *****	**0** ***** *****	**0** **A2** **B2**	**1** **A1** **B1**	**0** **A0** **B0**	Setup page start and end address A[2:0]: Page start address. Range: 0-7d B[2:0]: Page end address. Range: 0-7d	0 7d
Set Display Start Line	0	**40~7F**	**0**	**1**	**X5**	**X4**	**X3**	**X2**	**X1**	**X0**	Set display RAM display start line register from 0-63d.	0
Set Contrast Control	0	**81** **A[7:0]**	**1** **A7**	**0** **A6**	**0** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.	0x80
Set Brightness	0	**82** **A[7:0]**	**1** **A7**	**0** **A6**	**0** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**0** **A0**	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases.	0x80
Set Look-Up Table	0	**91** **X[5:0]** **A[5:0]** **B[5:0]** **C[5:0]**	**1** ***** ***** ***** *****	**0** ***** ***** ***** *****	**0** **X5** **A5** **B5** **C5**	**1** **X4** **A4** **B4** **C4**	**0** **X3** **A3** **B3** **C3**	**0** **X2** **A2** **B2** **C2**	**0** **X1** **A1** **B1** **C1**	**1** **X0** **A0** **B0** **C0**	Set current drive pulse width of Bank 0, Color A, B and C. Bank 0: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color A: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color B: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Color C: X[5:0] = 31 to 63. Pulse width set to 32 to 64 clocks. Note: Color D pulse width is fixed at 64 clocks.	0x31 0x3F 0x3F 0x3F
Set Bank Color of Bank1 to Bank16 (Page 0)	0	**92** **A[7:0]** **B[7:0]** **C[7:0]** **D[7:0]**	**1** **A7** **B7** **C7** **D7**	**0** **A6** **B6** **C6** **D6**	**0** **A5** **B5** **C5** **D5**	**1** **A4** **B4** **C4** **D4**	**0** **A3** **B3** **C3** **D3**	**0** **A2** **B2** **C2** **D2**	**1** **A1** **B1** **C1** **D1**	**0** **A0** **B0** **C0** **D0**	Sets the bank color of Bank1~Bank16 to any one of the 4 colors A,B,C, and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK1. A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK2. . . . D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK15. D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK16.	
Set Bank Color of	0	**93**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	Sets the bank color of Bank17~Bank32 to any one of the 4 colors	

Bank17 to Bank32 (Page 1)		**A[7:0]** **B[7:0]** **C[7:0]** **D[7:0]**	**A7** **B7** **C7** **D7**	**A6** **B6** **C6** **D6**	**A5** **B5** **C5** **D5**	**A4** **B4** **C4** **D4**	**A3** **B3** **C3** **D3**	**A2** **B2** **C2** **D2**	**A1** **B1** **C1** **D1**	**A0** **B0** **C0** **D0**	A,B,C, and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK17. A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK18. . . . D[5:4] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK31. D[7:6] : 00b, 01b, 10b, or 11b for Color = A, B, C, or D of BANK32.	
Set Segment Remap	0	**A0/A1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**X0**	X[0] = 0; Column address 0 is mapped to SEG0 X[0] = 1; Column address 131 is mapped to SEG0	0
Entire Display ON	0	**A4/A5**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**X0**	X[0] = 0; Resume RAM content display. Output follows RAM content. X[0] = 1; Entire display ON. Output ignores RAM content.	0
Set Normal/ Inverse Display	0	**A6/A7**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**X0**	X[0] = 0; Normal display. X[0] = 1; Inverse display.	0
Set Multiplex Ratio	0	**A8** **A[5:0]**	**1** *****	**0** *****	**1** **A5**	**0** **A4**	**1** **A3**	**0** **A2**	**0** **A1**	**0** **A0**	Set MUX ratio to N+1 MUX N=A[5:0]; from 16MUX to 64MUX (0 to 14 are invalid)	64
Dim mode setting	0	**AB** **A[3:0]** **B[7:0]** **C[7:0]**	**1** ***** **B7** **C7**	**0** ***** **B6** **C6**	**1** ***** **B5** **C5**	**0** ***** **B4** **C4**	**1** **A3** **B3** **C3**	**0** **A2** **B2** **C2**	**1** **A1** **B1** **C1**	**1** **A0** **B0** **C0**	A[3:0] = reserved. Set as 0000b B[7:0] = Set contrast for BANK0. Range 0-255d. Refer to command 81h. C[7:0] = Set brightness for color bank. Range 0-255d. Refer to command 82h.	
Master configuration	0	**AD** **AE**	**1** **1**	**0** **0**	**1** **0**	**0** **0**	**1** **1**	**1** **1**	**0** **1**	**1** **0**	Selects external VCC supply	AEh
Set Display ON/ OFF	0	**AC/** **AE/** **AF**	**1**	**0**	**1**	**0**	**1**	**1**	**A1**	**A0**	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) AFh = Display ON in normal mode	AEh
Set Page Start Address	0	**B0~B7**	**1**	**0**	**1**	**1**	**0**	**X2**	**X1**	**X0**	Set GDRAM Page Start Address for Page Addressing Mode using X[2:0]. PAGE0~PAGE7	
Set COM Output Scan Direction	0	**C0/C8**	**1**	**1**	**0**	**0**	**X3**	**0**	**0**	**0**	X[3] = 0; Normal mode. Scan from COM0 to COM[N-1] X[3] = 1; Remapped mode. Scan from COM[N-1] to COM0	0
Set Display Offset	0	**D3** **A[5:0]**	**1** *****	**1** *****	**0** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	Set vertical shift by COM from 0~63.	0
Set Display Clock Divide Ratio / Oscillator Frequency	0	**D5** **A[7:0]**	**1** **A7**	**1** **A6**	**0** **A5**	**1** **A4**	**0** **A3**	**1** **A2**	**0** **A1**	**1** **A0**	A[3:0] = Define the divide ratio of the display clocks. Divide ratio = A[3:0] +1 A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	0000b 0111b
Set Area Color Mode ON/OFF & Low Power Display Mode	0	**D8** **X[5:0]**	**1** **0**	**1** **0**	**0** **X5**	**1** **X4**	**1** **0**	**0** **X2**	**0** **0**	**0** **X0**	X[5:4] = 00b; Monochrome mode X[5:4] = 11b; Area Color mode X[2] = 0 and X[0] = 0; Normal power mode X[2] = 1 and X[0] = 1; Set low power display mode	00 00
Set Pre-charge Period	0	**D9** **A[7:0]**	**1** **A7**	**1** **A6**	**0** **A5**	**1** **A4**	**1** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	A[3:0] = Phase 1 period of up to 15 DCLK clocks. 0 is invalid. A[7:4] = Phase 2 period of up to 15 DCLK clocks. 0 is invalid.	2h 2h
Set COM pins Hardware configuration	0	**DA** **X[5:4]**	**1** **0**	**1** **0**	**0** **X5**	**1** **X4**	**1** **0**	**0** **0**	**1** **1**	**0** **0**	X[4] = 0; Sequential COM pin configuration X[4] = 1; Alternative COM pin configuration X[5] = 0; Disable COM Left/Right remap X[5] = 1; Enable COM Left/Right remap	1 1
Set VCOMH Deselect Level	0	**DB** **A[5:2]**	**1** **0**	**1** **0**	**0** **A5**	**1** **A4**	**1** **A3**	**0** **A2**	**1** **0**	**1** **0**	A[5:2] = 0000b; VCOMH = ~0.43*VCC A[5:2] = 1101b; VCOMH = ~0.77*VCC A[5:2] = 1111b; VCOMH = ~0.83*VCC	1101
Enter Read Modify Write mode	0	**E0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	Enter the Read/Modify/Write mode.	
NOP	0	**E3**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	Command for No Operation	
Exit Read Modify Write mode	0	**EE**	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**	Exit the Read/Modify/Write mode.	

For detailed instruction information, see SSD1305 datasheet .

MPU Interface

6800‐MPU Parallel Interface

The parallel interface consists of 8 bi‐directional data pins, R/W, D/C, E, and /CS.

A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.

A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.

The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

8080 - MPU Parallel Interface

The parallel interface consists of 8 bi - directional data pins, /RD, /WR, D/C, and /CS.
A LOW on D/C indicates “Command” read or write, and HIGH on D/C indicates “Data” read or write.
A rising edge of /RS input serves as a data read latch signal while /CS is LOW.
A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

Alternatively, /RD and /WR can be kept stable while /CS serves as the data/command latch signal.

Function	/RD	/WR	/CS	D/C
Write Command	1	0	↑	0
Read Status	0	1	↑	0
Write Data	1	0	↑	1
Read Data	0	1	↑	1

Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, and /CS.

D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	0	0	0	0	↑
Write Data	0	0	0	1	↑

SDIN is shifted into an 8 - bit shift register on every rising edge of SCLK in the order of D7, D6,…D0.
D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDRAM or command register in the same clock.
Note: Read is not available in serial mode.

I2C Interface

The I2C interface consists of a slave address bit SA0, I2C - bus data signal SDA, and I2C - bus clock signal SCL.

D1 and D2 can be tied together, and act as SDA. D0 acts as SCL. Both the data and clock signals must be connected to pull - up resistors. /RES is used to initialize the device.

Note: SA0 bit allows the device to have a slave address of either “0111100” or “0111101”.

Note: Data and acknowledgement are sent through the SDA. The ITO track resistance and the pull - up resistance at SDA becomes a voltage potential divider. As a result, it may not be possible to attain a valid logic
“0” level on SDA for the ACK signal. SDAIN must be connected, but SDAOUT may be disconnected and the ACK
signal will be ignored on the I2C bus.

12. Display Control Instructions

14 . DESIGN AND HANDING PRECAUTION

14.1 The LCD panel is made by glass. Any mechanical shock (eg. Dropping form high place) will damage the LCD module. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.

14.2 The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.

14.3 Never attempt to disassemble or rework the LCD module.
14.4 Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
14.5 When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
14.6 Ensure to provide enough space(with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result
14.7 Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
14.8 Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
14.9 LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
14.10 When peeling of the protective film form LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
14.11 Take care and prevent get hurt by the LCD panel edge.
14.12 Never operate the LCD module exceed the absolute maximum ratings.
14.13 Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
14.14 Never apply signal to the LCD module without power supply.
14.15 IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
14.16 LCD module reliability may be reduced by temperature shock.
14.17 When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module